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10/677,082	09/30/2003	Peter J. Barry	884.A79US1	4058

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EXAMINER	
ALROBAYE, IDRISS N	
ART UNIT	**PAPER NUMBER**
2183	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/677,082	BARRY, PETER J.	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to communications through the applicant's application filed on 02/26/2008.

2. Claims 1-25 presented for examination.

3. Applicant's amendment to the specification has been considered but did not completely overcome 35 USC 101 rejections (see response to arguments below).

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 18-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

6. As per claims 18-25, the claims recite "a machine-readable medium". Page 7, first paragraph of the specification provides intrinsic evidence that applicant's clear intent is that the broadest reasonable interpretation the claim term "machine readable media" is that the term is to encompass propagated signals. Propagated signals are a form of energy. Energy is not one of the four categories of invention and therefore the claims are not statutory. Energy is not a series of steps or acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or

manufacture. Energy is not a combination of substances and therefore is not a composition of matter. Accordingly, the rejection of claims 18-25 are non-statutory.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Baror et al. U.S. Patent No. 5,438,670 (hereinafter Baror).

9. As per claim 1, Baror teaches a method comprising:

commencing execution of a first set of one or more write instructions (Baror, abstract and col. 3, lines 30-46),

wherein the write instructions of the first set are the width of a processor data bus (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26; see also table 1);

aborting the execution of the first set of write instructions (Baror, col. 18, line 46 to col. 19, line, 'abort trap');

creating a second set of one or more write instructions, in response to the aborting, wherein the write instructions of the second set are the width of an expansion bus (Baror, col. 21 line 57 to col. 22, line 26; see also col. 27 lines 40-48; col. 18 line 46 to col. 19, line 4); and

executing the second set of write instructions (Baror, col. 21 line 57 to col. 22, line 26; see also table 1).

10. As per claim 2, Baror further teaches the method of claim 1, wherein the width of the processor bus is 32 bits (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

11. As per claim 3, Baror further teaches the method of claim 1, wherein the width of the expansion bus is 16 bits (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

12. As per claim 4, Baror further teaches the method of claim 1, wherein the second set of write instructions are suitable for transmission over the expansion bus (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

13. As per claim 5, Baror teaches a method comprising:

executing a write instruction that writes to a virtual memory address (Baror, abstract and col. 3, lines 30-46);

translating the virtual memory address (Baror, abstract and col. 3, lines 26-46),

wherein translating includes determining whether the virtual memory address maps to an inaccessible physical memory address (Baror, col. 18, line 46 to col. 19, lines 4);

generating an abort indication after determining that the virtual memory address maps to an inaccessible physical memory address (Baror, col. 18, line 46 to col. 19, line, 'abort trap');

performing the following in response to the abort indication, creating multiple write instructions suited for transmission over an expansion bus (Baror, col. 21 line 57 to col. 22, line 26); and

executing the multiple write instructions (Baror, col. 21 line 57 to col. 22, line 26).

14. As per claim 6, Baror further teaches the method of claim 5, wherein the expansion bus is 16 bit wide (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

15. As per claim 7, Baror further teaches the method of claim 6, wherein the write instruction is a 32-bit write instruction (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

16. As per claim 8, Baror further teaches the method of claim 6, wherein the write instruction is wider than the expansion bus (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 53).

17. As per claim 9, Baror teaches an apparatus comprising:

a memory management unit to receive a virtual address, the memory management unit to determine whether the virtual address maps to an inaccessible physical address and to transmit an abort indication if the virtual address maps to an inaccessible address (Baror, col. 18, line 46 to col. 19, line 4, 'MMU'); and

a processor core (Fig. 2) to receive the abort indication from the memory management unit and to execute instructions (Baror, col. 18, line 46 to col. 19, lines 4; see also, Fig. 3), the processor core including an abort handler to create new instructions in response to receipt of the abort indication (Baror, col. 27, lines 40-48; col. 18, line 46 to col. 19, line 4; col. 32, line 66 to col. 33, line 5), wherein the new instructions are the width of an expansion bus (Baror, col. 35, lines 1-2; col. 18, line 46 to col. 19, line 4; col. 21 line 57 to col. 22, line 26).

18. As per claim 10, Baror further teaches the apparatus of claim 9, wherein a physical address is inaccessible if it is write-protected (Baror, col. 18, line 46 to col. 19, lines 4).

19. As per claim 11, Baror further teaches the apparatus of claim 9 further comprising: an external expansion device communicatively coupled to the processor core, the external expansion device to receive the new instructions over the expansion bus (Fig. 2, and 3 and col. 18, line 46 to col. 19, lines 4; see also abstract).

20. As per claim 12, Baror further teaches the apparatus of claim 11, wherein the expansion bus is 16 bits wide (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

21. As per claim 13, Baror further teaches the apparatus of claim 9, wherein instructions are 32-bit instructions (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

22. As per claim 14, Baror teaches a system comprising:

a processor (Fig. 2), the processor including, processor core to receive an abort indication (Baror, col. 18, line 46 to col. 19, lines 4; see also, Fig. 3),

wherein the processor core includes an abort handler which in response to receipt of an abort indication is operable to create new write instructions suited for transmission over an expansion bus (Baror, col. 27, lines 40-48; col. 18, line 46 to col. 19, line 4; col. 32, line 66 to col. 33, line 5); and

a memory management unit (MMU) coupled to the processor core by a processor data bus (Baror, abstract and Fig. 3), the MMU to determine whether a virtual memory address maps to an accessible physical memory address (Baror, col. 18, line 46 to col. 19, line 4, 'MMU'), the MMU to transmit the abort indication to the processor core if the virtual memory address does not map to an accessible physical memory address (Baror, col. 18, line 46 to col. 19, line 4); an

external expansion device to receive the new write instructions from the processor over the expansion bus (Fig. 2, and 3 and col. 18, line 46 to col. 19, lines 4; see also abstract); and a dynamic random access memory (DRAM) unit coupled to the processor, wherein the DRAM unit is to store data accessible by the processor (Baror, Fig. 1, element 25 and col. 5, lines 13-24).

23. As per claim 15, Baror further teaches the system of claim 14, wherein the expansion bus is half the width of the processor data bus (Baror, col. 5, Table 1 and col. 21 line 57 to col. 22, line 26).

24. As per claim 16, Baror further teaches the system of claim 14, wherein the abort indication includes the virtual memory address (Baror, col. 18, line 46 to col. 19, lines 4 and abstract).

25. As per claim 17, Baror further teaches the system of claim 14, wherein the external expansion device is a flash memory device (Baror, Fig. 1, element 25 and col. 5, lines 13-24; see also abstract).

26. As per claims 18-21, they are rejected for the same reasons set forth above in claims 1-4.

27. As per claims 22-25, they are rejected for the same reasons set forth above in claims 5-8.

Response to Arguments

28. Applicant's arguments filed 02/26/2008 have been fully considered but they are not persuasive.

29. **Applicant's Argument**:

"*Claims 18-25 were rejected under 35 USC § 101 as being directed to non-statutory subject matter. In particular, the Office Action asserts that claims 18-25 are intended to encompass propagated signals. Applicant respectfully submits that there was no intent to claim non-statutory subject matter. Thus, Applicant has amended the specification as detailed above to remove the reference to the various forms of propagated signals in the first paragraph of page 7 as noted in the Office Action to clarify that only statutory subject mater was intended to be covered by the claims. Entry of the specification amendment and withdrawal of the 35 U.S.C. § 101 rejection is respectfully requested.*"

Examiner's Response:

The amendments to the specification is fine, however, the computer readable medium still encompasses transmission media. The specification still recites "*include machine-readable media for performing operations described herein. Machine-readable media includes any mechanism that provides (i.e., stores* ***and/or transmits****) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes*". The specification still refers to machine readable media to include mechanism that **transmits**. Therefore, to possibly overcome the 35 USC 101 rejections, the applicant must remove reference to media that transmits.

30. **Applicant's Argument**:

"*As stated above, Applicant respectfully traverses the rejections of claims 1-25 because Baror fails to teach the elements of the claims arranged in the manner as claimed. For example, independent claim 1 recites: "creating a second set of one or more write instructions, in response to the aborting." Emphasis added. In contrast, Baror, as cited in the Office Action does describe an abort and virtual to physical address translation, but fails to describe any actions taken in response to an abort. As a result, even if Baror were to disclose all of the elements, which Applicant does not admit, Baror fails to teach the elements of independent claim 1 arranged as in the claim. In particular, Baror fails to teach or suggest creating a second set of one or more write instructions in response to the aborting as arranged in independent claim 1.*"

Examiner's Response:

The examiner respectfully disagrees. The applicant admits that Baror teaches "**abort**" and as well known in the art, when an 'abort' occurs, there must be instructions proceeding aborting. Also, there must be instructions to recover from abort and the processor continues normal operation after aborting which meets the scope of the argued limitation "*creating a second set of one or more write instructions*"

Furthermore, Baror, col. 32, line 65 to col. 33, line 5 recites "*An abort trap occurs…In response to a trap (ABT), CPU 10 clears the P-flag in the current PSR before saving a copy and then forms…"* then the CPU performs normal operation afterwards which meets the scope of the claim. Also, col. 24, line 56 to col. 25, line 3 recites "*while in the state of processing an exception, CPU 10 is saving the PC, PSR, MOD contents and reading the PC and module linkage values to begin execution of exception service procedure".* This shows that there are instructions to process 'aborts'

or to recover from aborts and also there are instructions saved or written in response to occurrence of exception or aborting. Thus, reads on the argued claim limitation.

Therefore the argued claims stand as previously rejected.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

32. The following is text cited from 37 CFR 1.111(c): In amending reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent Application Publication No. 2004/0225840 shows method to provide multithreaded computer processing
- U.S. Patent No. 6,622,272 shows method for interfacing with external device.
- U.S. Patent No. 6,604,163 shows method for interconnection of digital signal processing with program memory and external devices using a shared bus interface.
- See also attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

IA